

FORM PTO-1449/A and B (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICATION NO.: 09/692,422	ATTY. DOCKET NO.: S1022.80545US00
		FILING DATE: October 19, 2000	CONFIRMATION NO.: 6731
		APPLICANT: Peter BALLAM	
		GROUP ART UNIT: 2125	EXAMINER: Albert William Paladini
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U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
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FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
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OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
Q4P		JOANNE E. DEGROAT, Transparent Logic Modeling in VHDL, IEEE Design & Test of Computers, US, IEEE Computers Society, Los Alamitos, vol. 7, no. 3, June 1, 1990, pages 42-48, XP000205089	

EXAMINER ALBERT W. PALADINI PATENT EXAMINER	DATE CONSIDERED 4-13-05
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*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. __, filed __, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

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